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Notice of Allowability	Application No.	Applicant(s)
	09/756,864	TANAKA ET AL.
	Examiner	Art Unit
	Thomas L Dickey	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTO-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

- This communication is responsive to request for RCE filed 8/4/03
- The allowed claim(s) is/are 15,16,21,24 and 25.
- The drawings filed on 10 January 2001 are accepted by the Examiner.
- Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - All
 - Some*
 - None of the.
 - Certified copies of the priority documents have been received.
 - Certified copies of the priority documents have been received in Application No. 09/095,612.
 - Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.
- Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - The translation of the foreign language provisional application has been received.
- Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. CORRECTED DRAWINGS must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1 hereto or 2 to Paper No. _____.
 - (b) including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
 - (c) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.

9. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| <input type="checkbox"/> Notice of References Cited (PTO-892) | <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | <input type="checkbox"/> Interview Summary (PTO-413), Paper No. _____. |
| <input type="checkbox"/> Information Disclosure Statements (PTO-1449), Paper No. _____. | <input type="checkbox"/> Examiner's Amendment/Comment |
| <input checked="" type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | <input type="checkbox"/> Other |

*Minhloan Tran
Minhloan Tran
Primary Examiner
Art Unit 2826*

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

Claims 15,16,21,24 and 25 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device comprising a memory cell region and a peripheral circuit region, a semiconductor substrate having a major surface; an insulating film, having an upper surface, being formed on said major surface of said semiconductor substrate to extend from said memory cell region to said peripheral circuit region, wherein said insulating film includes an upper insulating film and lower insulating film being different in etching rate from each other, a capacitor lower electrode assembly, including first and second lower electrodes being adjacent to each other through a part of said insulating film, being formed on said major surface of said semiconductor substrate to extend up to a vertical position substantially identical to that of said upper surface of said insulating film in said memory cell region; first and second openings formed in the insulating film, and the first and the second lower electrodes formed within the first and second openings, respectively; said first and second lower electrodes each of a cylindrical shape having an interior region; wherein respective sidewalls of the first and the second lower electrodes are formed to extend in a longitudinal direction with respect to the major surface of the semiconductor substrate, each sidewall having a cross-section in the longitudinal direction which is substantially linear; and a capacitor upper electrode being formed on said capacitor lower electrode assembly through a dielectric film to extend

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onto said upper surface of said insulating film, said upper electrode being formed on the interior region of each of the first and second electrodes, said capacitor lower electrode assembly including a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface and a bottom surface, further comprising granular crystals on a surface of said capacitor lower electrode, as recited in claim 16, or a semiconductor device comprising a memory cell region and a peripheral circuit region, a semiconductor substrate having a major surface; an insulating film, having an upper surface, being formed on said major surface of said semiconductor substrate to extend from said memory cell region to said peripheral circuit region, wherein said insulating film includes an upper insulating film and lower insulating film being different in etching rate from each other, a capacitor lower electrode assembly, including first and second lower electrodes being adjacent to each other through a part of said insulating film, being formed on said major surface of said semiconductor substrate to extend up to a vertical position substantially identical to that of said upper surface of said insulating film in said memory cell region; first and second openings formed in the insulating film, and the first and the second lower electrodes formed within the first and second openings, respectively; said first and second lower electrodes each of a cylindrical shape having an interior region; wherein respective sidewalls of the first and the second lower electrodes are formed to extend in a longitudinal direction with respect to the major surface of the semiconductor substrate, a capacitor upper electrode being formed on said capacitor lower electrode assembly through a dielectric

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film to extend onto said upper surface of said insulating film, said upper electrode being formed on the interior region of each of the first and second electrodes, said capacitor lower electrode assembly including a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface and a bottom surface, wherein a side surface of said capacitor lower electrode has a curved plane; and a first width of the first and second lower electrodes at their upper ends is narrower than a second width in a central portion, in the height direction, of the first and second lower electrodes, as recited in claim 25.

Takaishi 5,604,696 discloses a semiconductor device including a memory cell region 'X' and a peripheral circuit region 'Y', comprising: a semiconductor substrate 1 having a major surface, an insulating film 21-8, having an upper surface, being formed on the major surface of the semiconductor substrate 1 to extend from the memory cell region 'X' to the peripheral circuit region 'Y', a capacitor lower electrode assembly (part 22 generally), including first and second lower electrodes 22 being adjacent to each other through a part of the insulating film 21, being formed on the major surface of the semiconductor substrate 1 to extend up to a vertical position substantially identical to that of the upper surface of the insulating film 21 in the memory cell region 'X', first and second openings formed in the insulating film 21, and the first and the second lower electrodes 22 formed within the first and second openings, respectively, the first and second lower electrodes 22 each of a cylindrical shape having an interior region, wherein respective sidewalls of the first and the second lower electrodes 22 are formed

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to extend in a longitudinal direction with respect to the major surface of the semiconductor substrate 1, each sidewall having a cross-section in the longitudinal direction that is substantially linear, and a capacitor upper electrode 24 being formed on the capacitor lower electrode assembly through a dielectric film 23 to extend onto the upper surface of the insulating film 21-8, the upper electrode 24 being formed on the interior region of each of the first and second electrodes 22, the capacitor lower electrode assembly including a capacitor lower electrode part 22 upwardly extending in opposition to the capacitor upper electrode 24 and having a top surface and a bottom surface, wherein the insulating film 21-8 includes an upper insulating film 21 and a lower insulating film 8 being different in etching rate from each other. Note figures 4I and 4A of Takaishi. Wang et al. 5,856,220 discloses a semiconductor device including first and second capacitor lower electrodes whose side surfaces have curved plane; and a first width of the first and second lower electrodes at their upper ends is wider than a second width in a central portion, in the height direction, of the first and second lower electrodes. Note figure 12 of Wang et al. Neither Takaishi nor Wang discloses nor suggests (such suggestion necessarily requiring motivation for substitution) making the first and second lower electrodes at their upper ends narrower instead of wider (as disclosed by Wang) than in their central portions.

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

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accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Tues-Friday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

dd
10/2003